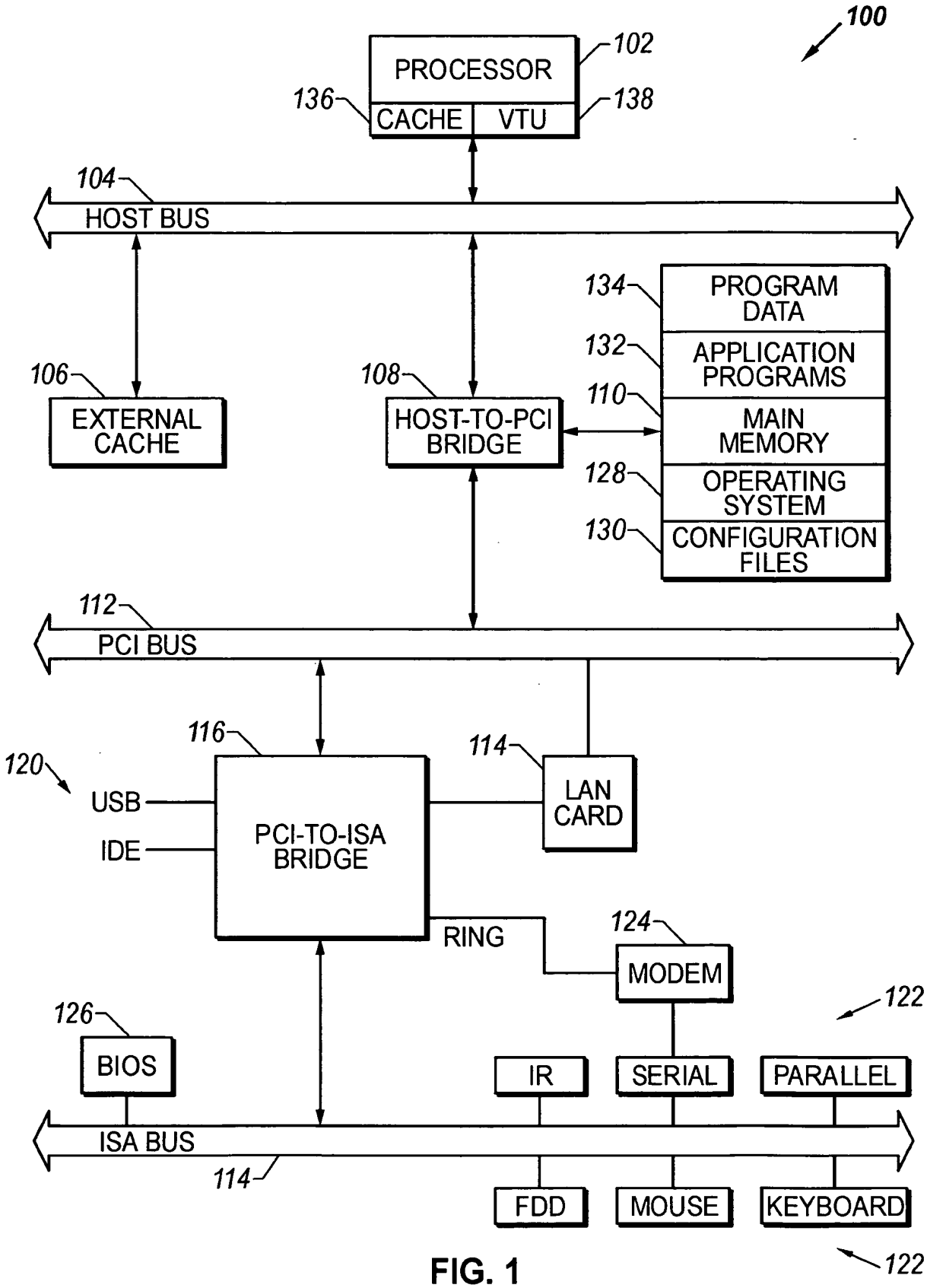
100
PROCESSOR
102
136
CACHE
VTU
138
104
HOST BUS
134
PROGRAM DATA
132
APPLICATION PROGRAMS
106
108
110
EXTERNAL CACHE
HOST-TO-PCI BRIDGE
MAIN MEMORY
128
OPERATING SYSTEM
130
CONFIGURATION FILES
112
PCI BUS
116
114
120
USB
IDE
PCI-TO-ISA BRIDGE
LAN CARD
RING
124
MODEM
122
126
BIOS
IR
SERIAL
PARALLEL
ISA BUS
114
FDD
MOUSE
KEYBOARD
122

FIG. 1

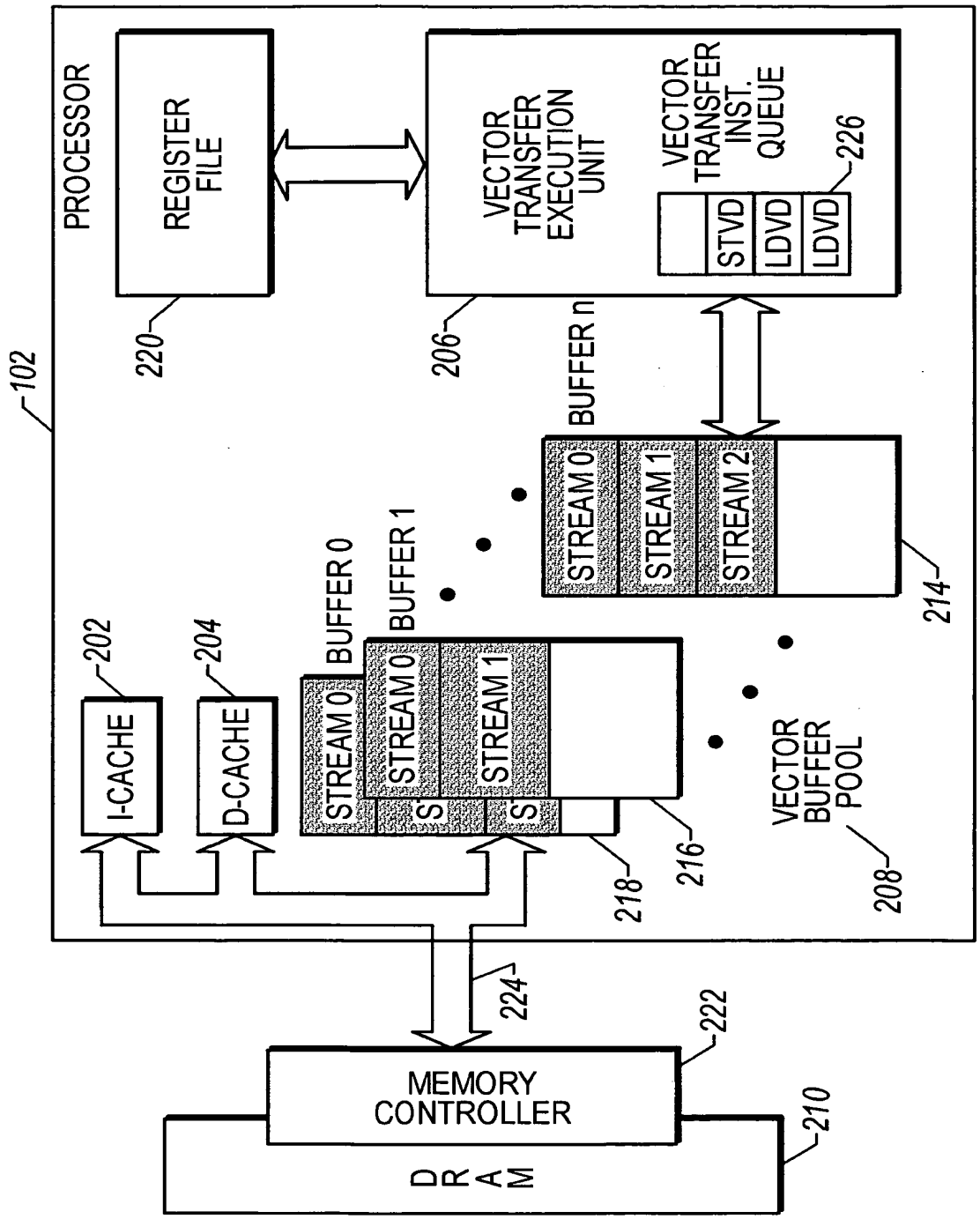
PROCESSOR
REGISTER FILE
VECTOR TRANSFER EXECUTION UNIT
VECTOR TRANSFER INST. QUEUE
STVD
LDVD
LDVD
226
220
206
102
BUFFER n
STREAM 0
STREAM 1
STREAM 2
214
BUFFER 0
BUFFER 1
STREAM 0
STREAM 0
STREAM 1
202
204
I-CACHE
D-CACHE
218
216
VECTOR BUFFER POOL
208
224
222
MEMORY CONTROLLER
DRAM
210

FIG. 2

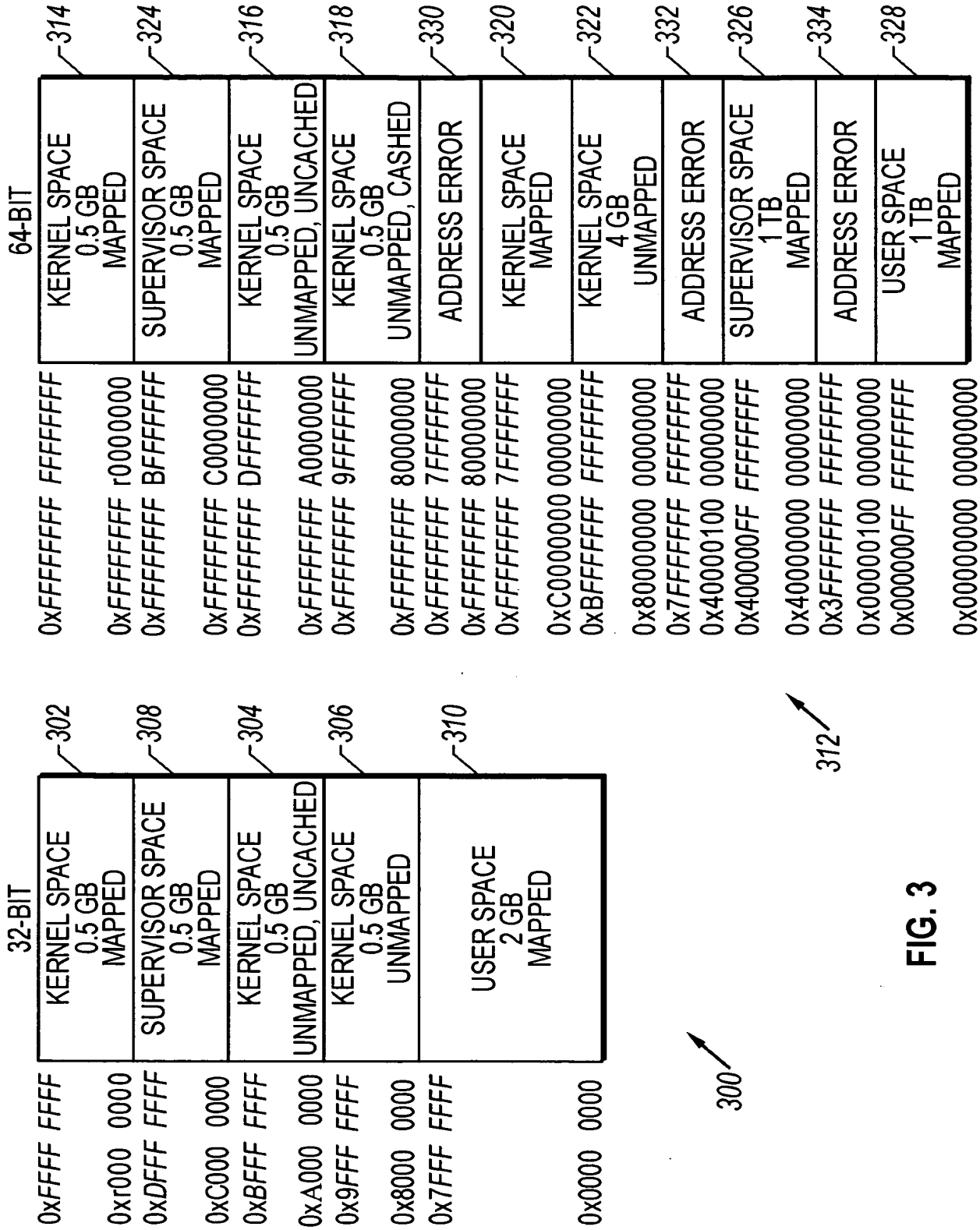
32-BIT
KERNEL SPACE 0.5 GB MAPPED
SUPERVISOR SPACE 0.5 GB MAPPED
KERNEL SPACE 0.5 GB UNMAPPED, UNCACHED
KERNEL SPACE 0.5 GB UNMAPPED
USER SPACE 2 GB MAPPED
0xFFFF FFFF
0xr000 0000
0xDFFF FFFF
0xC000 0000
0xBFFF FFFF
0xA000 0000
0x9FFF FFFF
0x8000 0000
0x7FFF FFFF
0x0000 0000
302
308
304
306
310
300
64-BIT
KERNEL SPACE 0.5 GB MAPPED
SUPERVISOR SPACE 0.5 GB MAPPED
KERNEL SPACE 0.5 GB UNMAPPED, UNCACHED
KERNEL SPACE 0.5 GB UNMAPPED, CASHED
ADDRESS ERROR
KERNEL SPACE MAPPED
KERNEL SPACE 4 GB UNMAPPED
ADDRESS ERROR
SUPERVISOR SPACE 1 TB MAPPED
ADDRESS ERROR
USER SPACE 1 TB MAPPED
0xFFFFFFFF FFFFFFFF
0xFFFFFFFF r0000000
0xFFFFFFFF BFFFFFFF
0xFFFFFFFF C0000000
0xFFFFFFFF DFFFFFFF
0xFFFFFFFF A0000000
0xFFFFFFFF 9FFFFFFF
0xFFFFFFFF 80000000
0xFFFFFFFF 7FFFFFFF
0xFFFFFFFF 80000000
0xFFFFFFFF 7FFFFFFF
0xC0000000 00000000
0xBFFFFFFF FFFFFFFF
0x80000000 00000000
0x7FFFFFFF FFFFFFFF
0x40000100 00000000
0x400000FF FFFFFFFF
0x40000000 00000000
0x3FFFFFFF FFFFFFFF
0x00000100 00000000
0x000000FF FFFFFFFF
0x00000000 00000000
314
324
316
318
330
320
322
332
326
334
328
312

FIG. 3

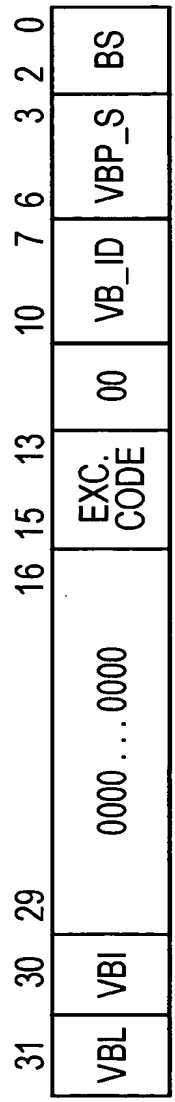
31
30
29
16
15
13
10
7
6
3
2
0
VBL
VBI
0000 . . . 0000
EXC. CODE
00
VB_ID
VBP_S
BS

FIG. 4

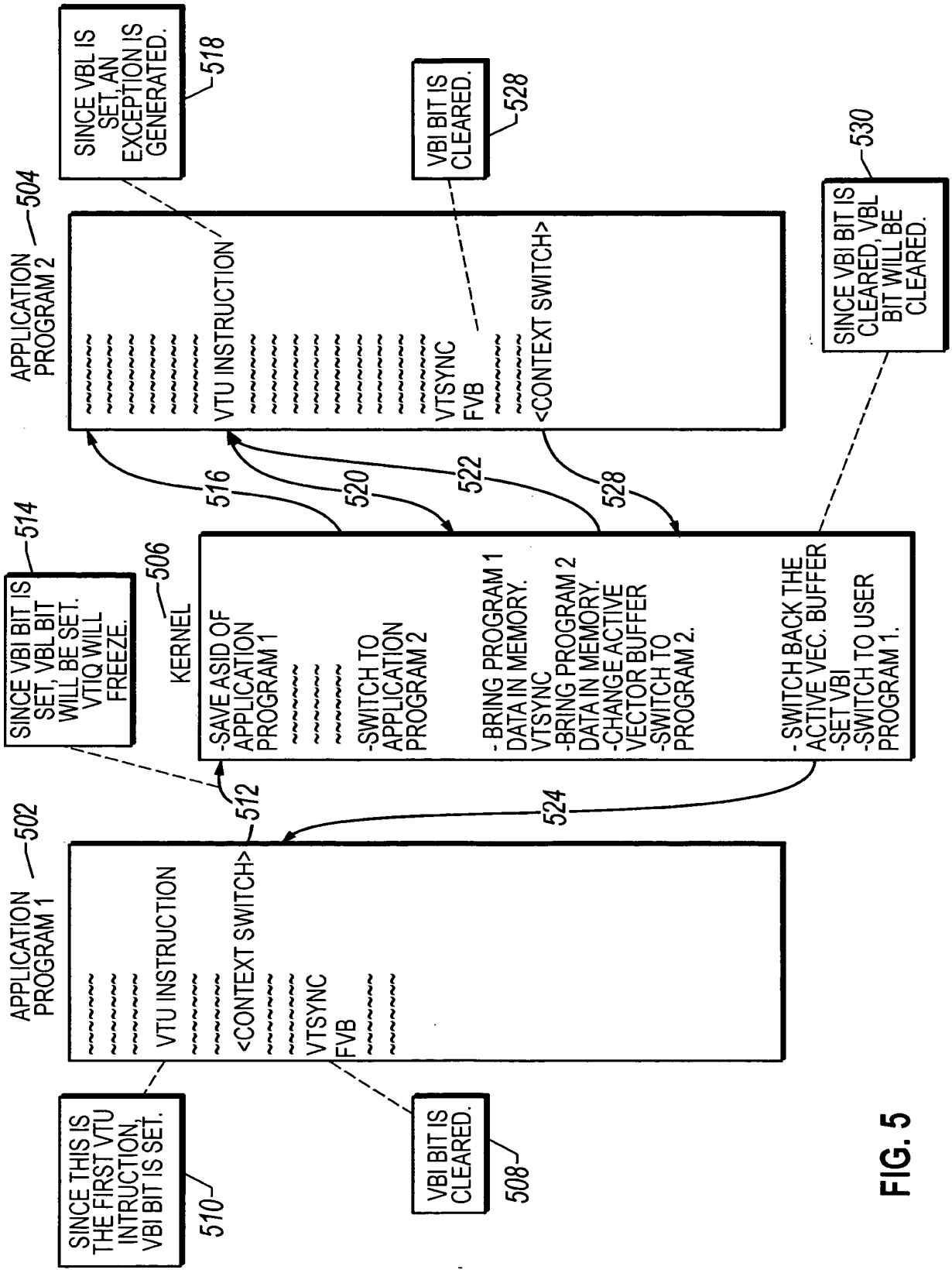
SINCE VBL IS SET, AN EXCEPTION IS GENERATED.
518
VBI BIT IS CLEARED.
528
530
SINCE VBI BIT IS CLEARED, VBL BIT WILL BE CLEARED.
APPLICATION PROGRAM 2
504
VTU INSTRUCTION
VTSYNC
FVB
<CONTEXT SWITCH>
516
520
522
528
514
SINCE VBI BIT IS SET, VBL BIT WILL BE SET. VTIQ WILL FREEZE.
506
KERNEL
-SAVE ASID OF APPLICATION PROGRAM 1
-SWITCH TO APPLICATION PROGRAM 2
- BRING PROGRAM 1 DATA IN MEMORY.
VTSYNC
-BRING PROGRAM 2 DATA IN MEMORY.
-CHANGE ACTIVE VECTOR BUFFER
-SWITCH TO PROGRAM 2.
- SWITCH BACK THE ACTIVE VEC. BUFFER
-SET VBI
-SWITCH TO USER PROGRAM 1.
512
524
APPLICATION PROGRAM 1
502
VTU INSTRUCTION
<CONTEXT SWITCH>
VTSYNC
FVB
SINCE THIS IS THE FIRST VTU INTRUCTION, VBI BIT IS SET.
510
VBI BIT IS CLEARED.
508

FIG. 5

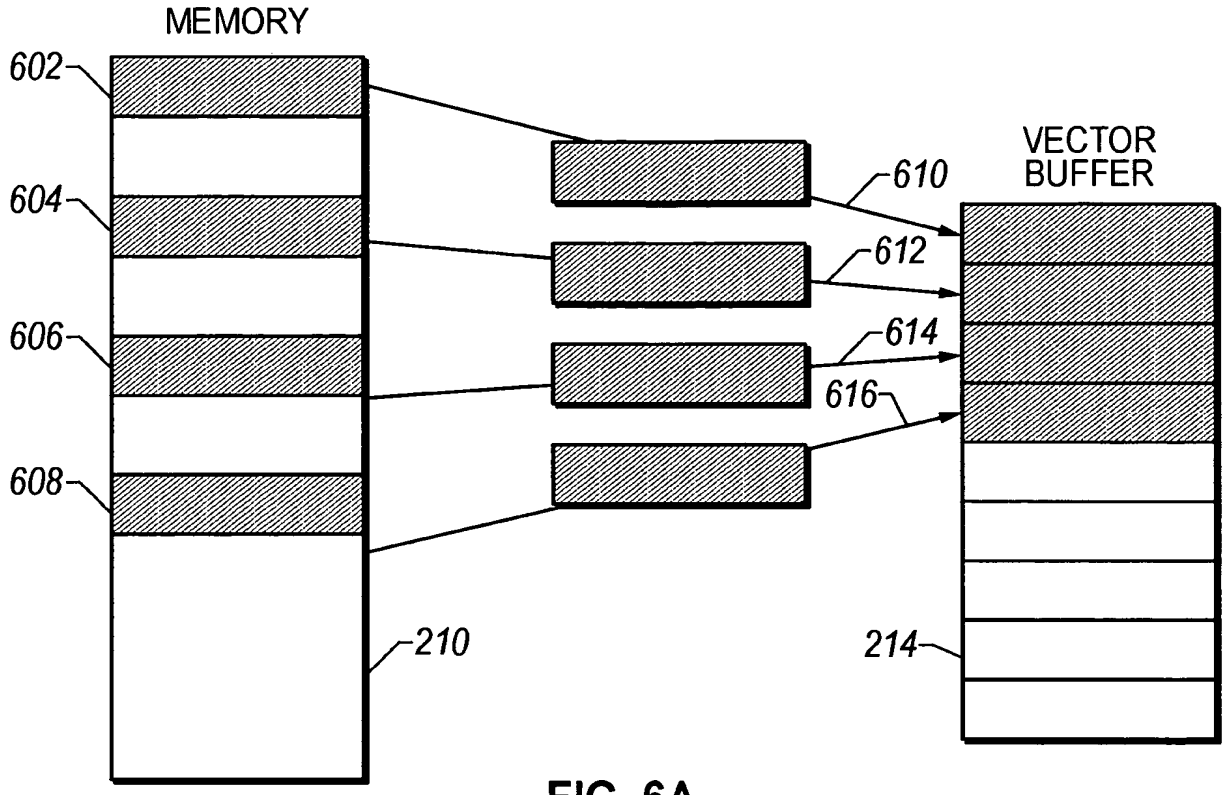
MEMORY
602
604
606
608
210
610
612
614
616
VECTOR BUFFER
214

FIG. 6A

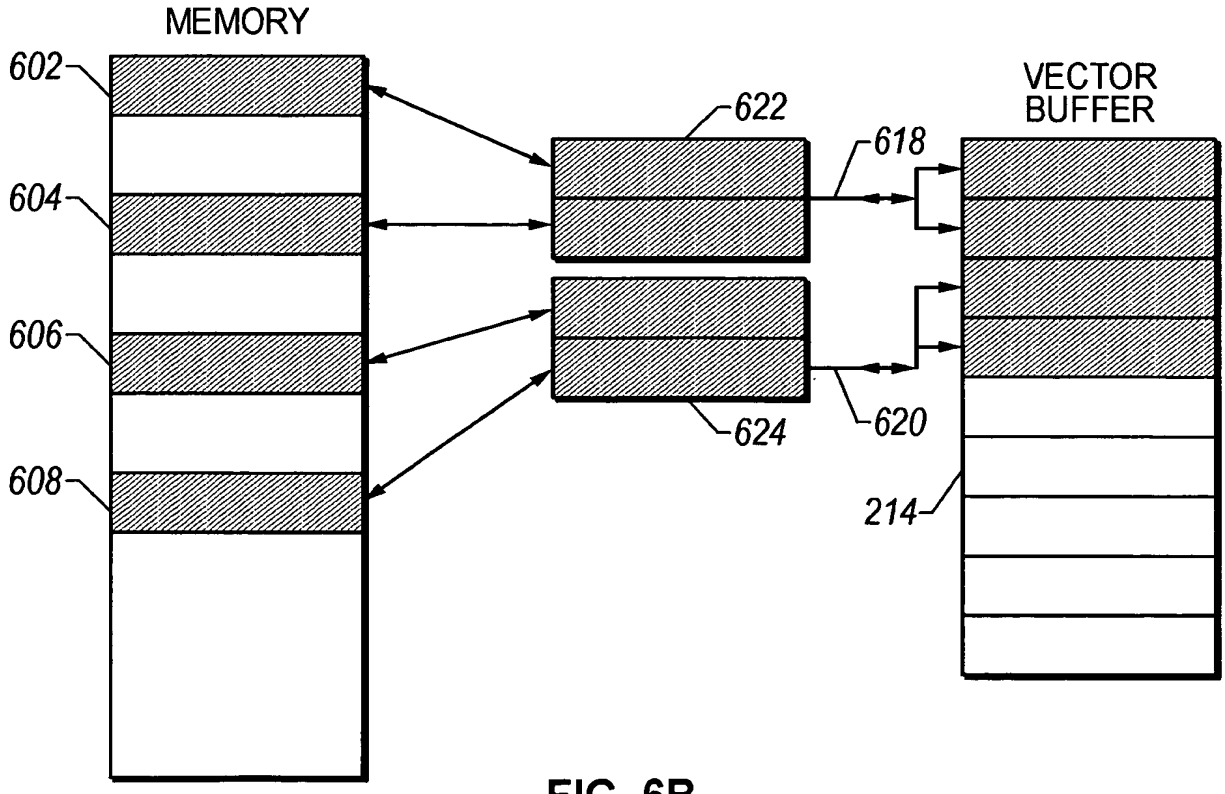
MEMORY
602
604
606
608
622
624
618
620
VECTOR BUFFER
214

FIG. 6B

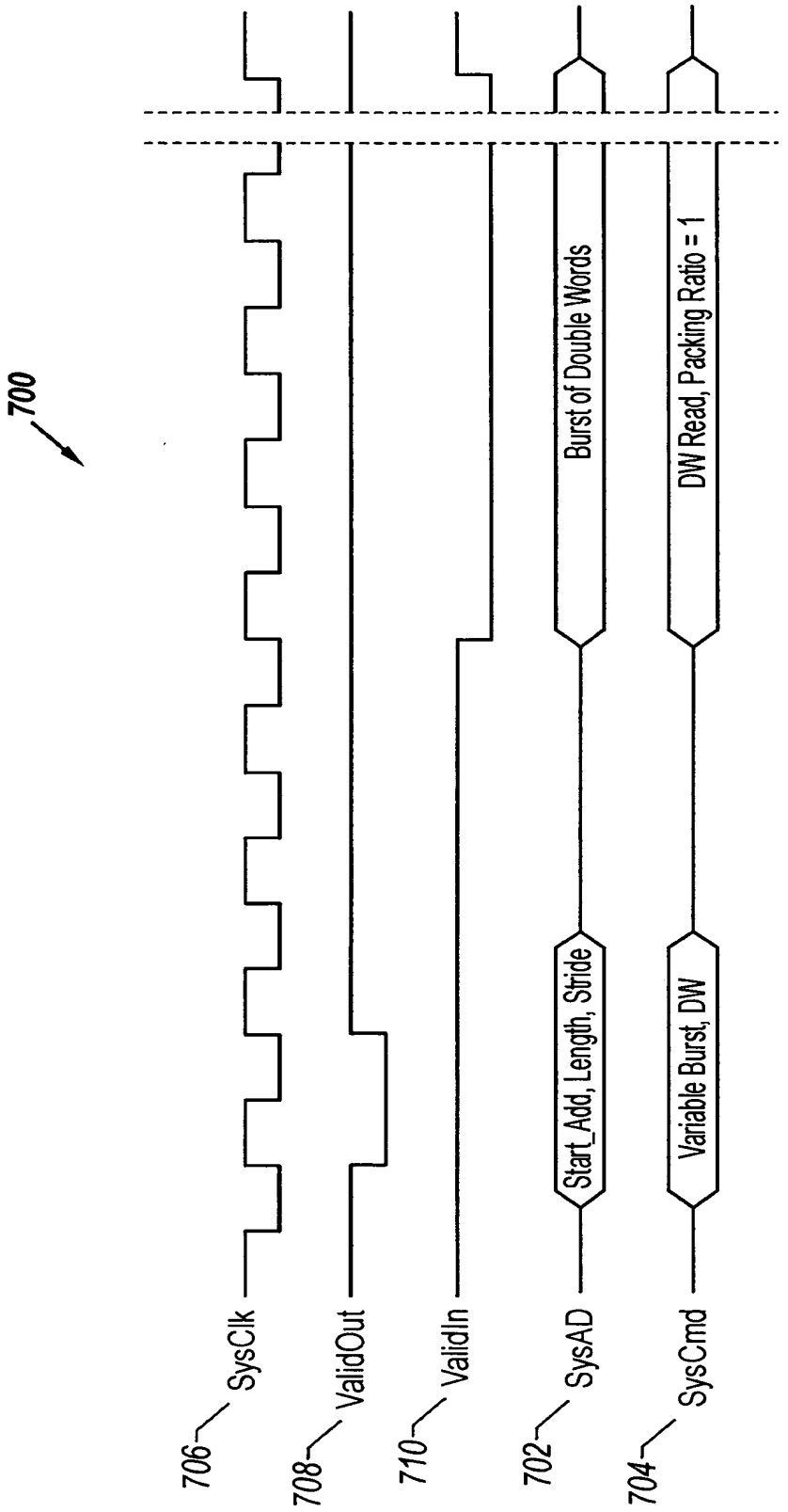
700
SysClk
706
ValidOut
708
ValidIn
710
SysAD
702
SysCmd
704
Start_Add, Length, Stride
Variable Burst, DW
Burst of Double Words
DW Read, Packing Ratio = 1

FIG. 7

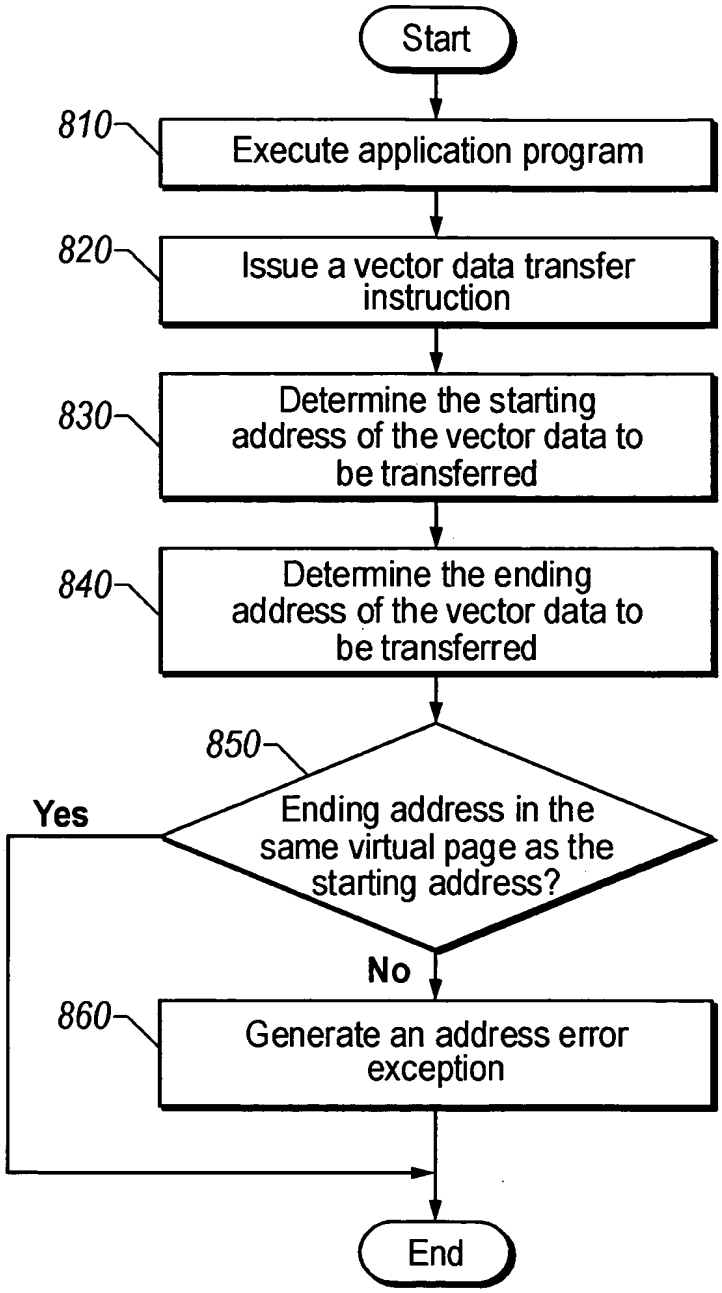
Start
810
Execute application program
820
Issue a vector data transfer instruction
830
Determine the starting address of the vector data to be transferred
840
Determine the ending address of the vector data to be transferred
850
Ending address in the same virtual page as the starting address?
Yes
No
860
Generate an address error exception
End

FIG. 8